

AMENDMENTS TO THE SPECIFICATION

Please delete the last four paragraphs of page 3.

Please delete all of page 4.

Please delete all of page 5.

Please amend the first paragraph of page 6 as follows:

~~Still further, according to the invention, there is provided a method of forming a zener zap diode device, comprising forming a first polysilicon layer on a n-type silicon, n-doping the first polysilicon layer, forming a second polysilicon layer on the n-type silicon, spaced from the first polysilicon layer, p-doping the second polysilicon layer, depositing a refractory metal layer on at least part of the second polysilicon layer, reacting the refractory metal with silicon to form a silicide, and establishing a current between the first and second polysilicon layers to create a silicided bridge formed from the metal silicide to form a low resistance path between contacts to the first and second polysilicon layers, wherein the steps are performed in an order suitable for a double poly process. Again, the polarities of the structures and dopants could instead be opposite to those described above.~~

B' A semiconductor device in accordance with the present invention includes a buried layer that has a first conductivity type, and an epitaxial region that is formed on the buried layer. The epitaxial region has a surface and includes a first region and a second region. The first region, which has a first conductivity type, contacts the buried region and the surface. The second region, which has a second conductivity type, contacts the surface and the first region. The second region includes all contiguous regions that have the second conductivity type. In addition,

no region of a first conductivity type is enclosed between the second region and the surface.

The semiconductor device also includes a first conductor that is formed on the surface to make an electrical connection with the first region, and a second conductor that is formed on the surface. The second conductor contacts the second region, and is spaced apart from the first conductor.

A semiconductor device in further accordance with the present invention includes a semiconductor material that has a surface. The semiconductor material includes a first region of a first conductivity type that contacts the surface, and a second region of a second conductivity type that contacts the surface and the first region.

B' The second region includes all contiguous regions that have the second conductivity type. No region of a first conductivity type is enclosed between the second region and the surface. The first region includes a third region that lies vertically below all of the second region, has the first conductivity type, and has a substantially uniform dopant concentration.

The semiconductor device further includes a first conductor that is formed on the surface to make an electrical connection with the first region. The first conductor has the first conductivity type and a dopant concentration. The dopant concentration of the third region and the dopant concentration of the first conductor are substantially equal.

The semiconductor device additionally includes a second conductor that is formed on the surface. The second conductor contacts the second region, has the second conductivity type, and is spaced apart from the first conductor.

The present invention also includes a method of operating a semiconductor device that includes the steps of applying a first voltage to the first conductor, and applying a second voltage to the second conductor. The first and second voltages causing a reverse breakdown of a junction between the first region and the second

B1 region such that metal atoms from the layer of metal silicide migrate to form a metallic path through the junction.

Please amend the last paragraph of page 6 (which continues onto page 7) as follows:

B2 Figure 5 shows an example of a device comprising a an n-buried layer (NBL) 50 formed in a substrate. An n-epitaxial or n+ sinker region 52 is formed on n-buried layer 50. Region 52, in turn, is isolated from laterally adjacent regions by isolation region 53. Two polysilicon layers are formed in a on n-epitaxial or n+ sinker region 52 in creating the device: a first poly layer 54, and a second poly layer 56. In this embodiment, the first poly layer 54 is formed first and is therefore depicted as poly 1, while the second poly layer is formed after the first poly layer 54 and is therefore depicted as poly 2. The second poly layer 56 is n-doped to form a n+ emitter an n+ region 58 in the n-epitaxial or n+ sinker region 52 at the same time that other second poly layers are doped to form, for example, n+ emitters. The first poly layer 54 comprises two portions which are oppositely doped in this embodiment. A first portion 62 of the first polysilicon layer 54 is p-doped to form a p-extrinsic base (PXB) p+ region 64 in the n-epitaxial region or n+ sinker 52 at the same time that other first polysilicon layers are p-doped to form, for example, the p-extrinsic bases of npn transistors. A second portion 68 of the first polysilicon layer 54 is n-doped to define a n-extrinsic base (NXB) an n+ region 70 in the n-epitaxial or n+ sinker region 52 at the same time that other first polysilicon layers are n-doped to form, for example, the n-extrinsic bases of pnp transistors. A p-n junction is established in this embodiment by the PXB p+ region 64 and the n-epitaxial or n-sinker n+ sinker region 52 which is contacted through the NXB n+ region 70 and the n-doped poly 1 portion 68.

Please amend the first full paragraph on page 7 as follows:

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Figure 5, further shows a silicided refractory metal layer 80 which, in this case, is a Cobalt silicide layer. In practice, Cobalt or ~~other~~ another refractory metal is blanket deposited on the device and thereafter reacted at elevated temperatures with the silicon to form the silicide. The unreacted Cobalt or other refractory metal is then etched off leaving only the areas of Cobalt silicide on the polysilicon areas. The silicide at this point in the process is often referred to as silicide. As can be seen in Figure 5, the Cobalt silicide layer is formed on top of the first and second polysilicon layers but does not extend over the oxide dielectric 82. In this way the ~~bipolar junction is maintained~~ oxide dielectric 82 prevents the Cobalt silicide from shorting out the p-n junction prematurely. As can be seen, the regions 62 and 68 are also isolated from the second polysilicon region 56 by the nitride spacers 84. However, a ~~lower~~ low resistance path is ~~created by the n+ emitter facilitated by n+ region 58~~. Thus, when the device is reverse biased by applying a voltage across the contacts 90, which in this embodiment comprise aluminum contacts formed in titanium nitride (TiN) sleeves 94, a fusing current is established which heats the p-n junction and causes the Cobalt silicide to migrate across the p-n junction to form a silicide bridge, in this case a Cobalt silicide bridge. Thus, by using standard process steps in a double poly process and ~~configuring the spacing of the bipolar junction~~ and modifying the resistance path across the ~~junction~~ n-epitaxial or n-sinker region 52, Cobalt or another refractory metal can be used to establish a silicide bridge across the p-n junction thereby effectively shorting out the p-n junction. Thus, the present invention allows the device to be used as a zener zap diode.

Please amend the last paragraph of page 7 (which continues onto page 8) as follows:

Another embodiment of the invention is illustrated in the Figure 6 example showing a device comprising a an n-buried layer (NBL) 50 formed in a substrate. An n-epitaxial or n+ sinker region 114 is formed on n-buried layer 50. Region 114, in turn, is isolated from laterally adjacent regions by isolation region 115. Two polysilicon layers are formed in a on n-epitaxial or n+ sinker region 114 in creating the device. The first polysilicon layer (poly 1) 100 is used to form ~~a n-extrinsic base (NXB)~~ an n+ region 102. The second polysilicon layer (poly 2) 104 includes a p-doped region 106 and a an n-doped portion 108. The two polysilicon regions 106 ; and 108 form a p+ region 110 and a an n+ region 112, respectively, in a n-epitaxial or ~~n-sinker~~ n+ sinker region 114. The p+ region 110 and n+ region 112 ~~define either emitters,~~ can be formed, for example, when the emitters of other transistors are formed in the case of bipolar devices, or when the drains and sources of MOS transistors are formed in the case of MOS devices. A p-n junction is established in this embodiment by the p+ region 110 and the n-epitaxial or ~~n-sinker~~ n+ sinker region 114 which is contacted through the n+ region 112 and the n-doped poly 2 portion 108. Again, the poly 2 portions 106 ; and 108 are spaced from the poly 1 layer 100 by means of nitride spacers 120. The Cobalt silicide or other silicided refractory metal 122 extends across the first and second poly layers 100 ; and 104 ~~but maintains the bipolar junction by~~ . By virtue of the oxide dielectric 124, the Cobalt silicide is prevented from shorting out the p-n junction prematurely. Again, a silicide bridge can be established across the p-n junction by migrating the Cobalt silicide atoms across the p-n junction from the p-doped poly 2 portion 106 to the n-doped poly 2 portion 108.

Please amend the first full paragraph on page 8 (which continues over to page 9) as follows:

Figure 7 shows an example of yet another embodiment of the invention. A An n-tub in the form of a n-epitaxial or ~~n-sinker~~ n+ sinker region 250 is bounded on its lower surface by a n-buried layer (NBL) 252 and on its sides by oxide regions 254. In this embodiment the first formed polysilicon layer (poly 1) 260 is n-doped to ~~define a n-extrinsic base (NXB)~~ form an n+ region 262 in the tub 250. The second formed polysilicon layer 264 is p-doped to form a p+ region 266 in the tub 250. The p+ region could be formed when, for example, an emitter is formed, in the case of a bipolar device, or when a source or drain is formed in the case of a MOS device. The second formed polysilicon layer 264 (poly 2) is spaced from the poly 1 region 260 by a nitride spacer 270 ; to define a p-n junction between the p+ region 266 and the n-epitaxial or ~~n-sinker~~ n+ sinker region 250 which is contacted through the ~~NXB~~ n+ region 262 and n-doped poly 1 layer 260. A Cobalt silicide layer 274 or other silicided refractory metal is formed on top of the polysilicon layers 264 ; and 260. Again an oxide region, in this case oxide region 280, prevents the Cobalt silicide from shorting out the p-n junction prematurely. Again, this device can be used as an anti-fuse in accordance with the invention by selectively shorting out the p-n junction by applying a reverse voltage across the p-n junction to cause ~~electron~~ electrons to flow from the p+ polysilicon region 264 to the n+ polysilicon region 260 thereby causing Cobalt silicide atoms to migrate across the junction to form a Cobalt silicide bridge that shorts out the p-n junction. It will be appreciated that the Cobalt silicide layer need only be formed on the p+ polysilicon region 264, however, a typical process will usually form the Cobalt silicide on both polysilicon layers 264 ; and 260. This also has the advantage that the silicide bridge need only extend from the cobalt silicide layer on the p+ polysilicon region to the cobalt silicide layer on the n+ polysilicon region instead of all the way to the actual contact. Thus, the length

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85 of the bridge is reduced, which is one of the considerations of the invention in providing a configuration that will allow a bridge to be formed under sufficiently low zap currents so as to avoid unwanted damage to the structure.

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